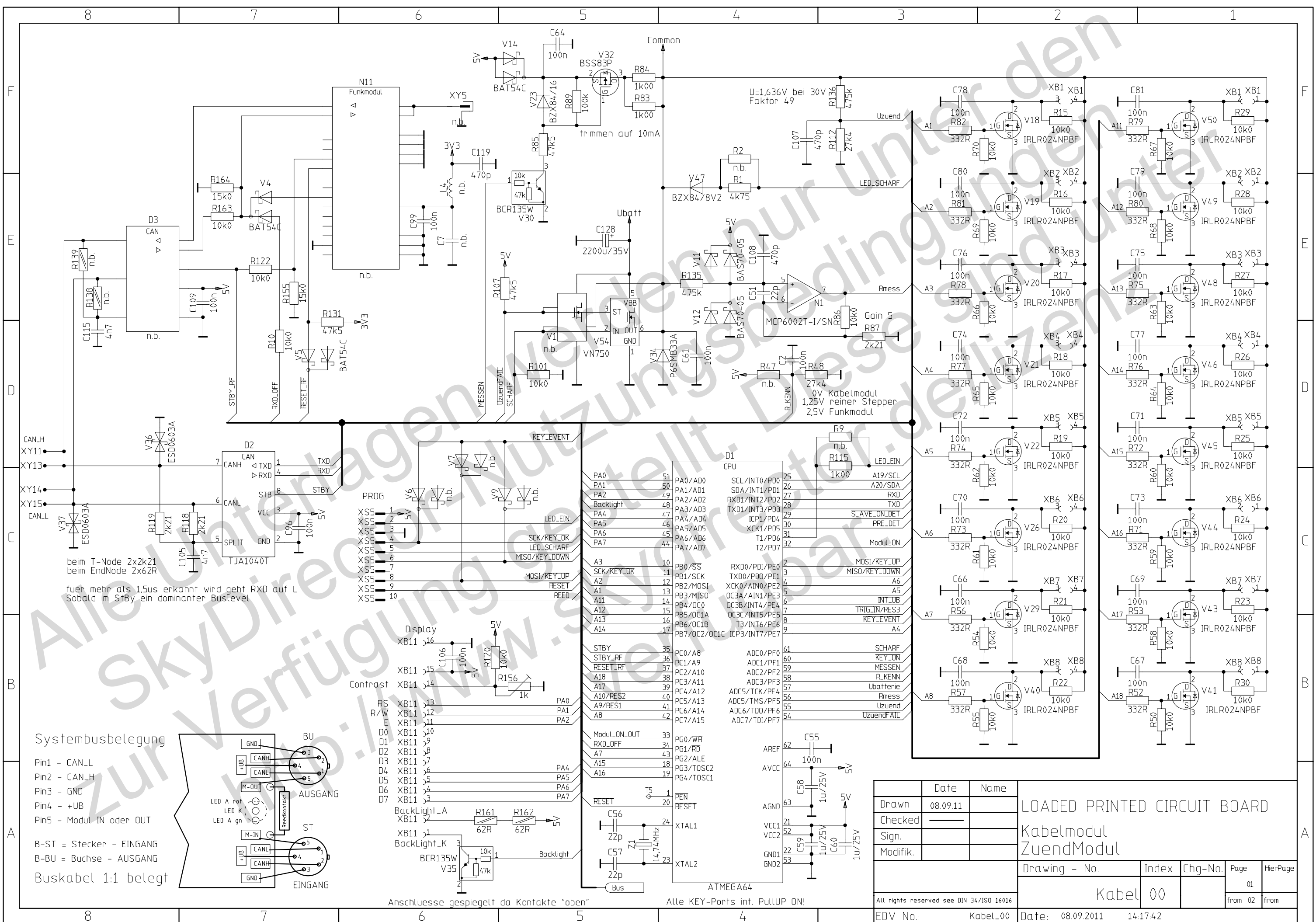
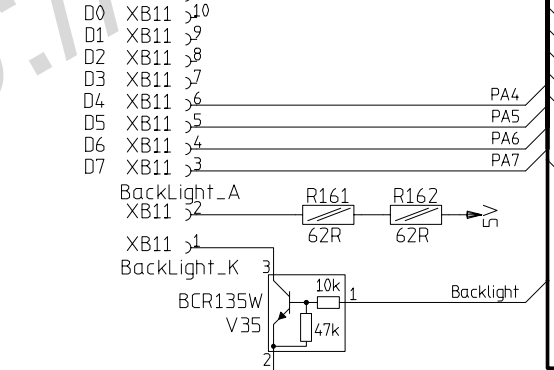
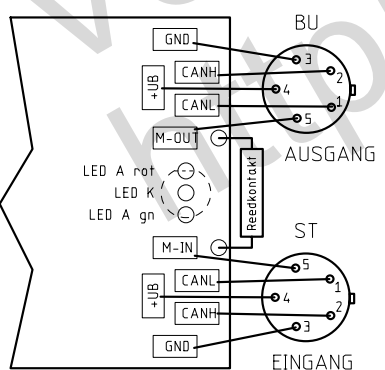




Systembusbelegung

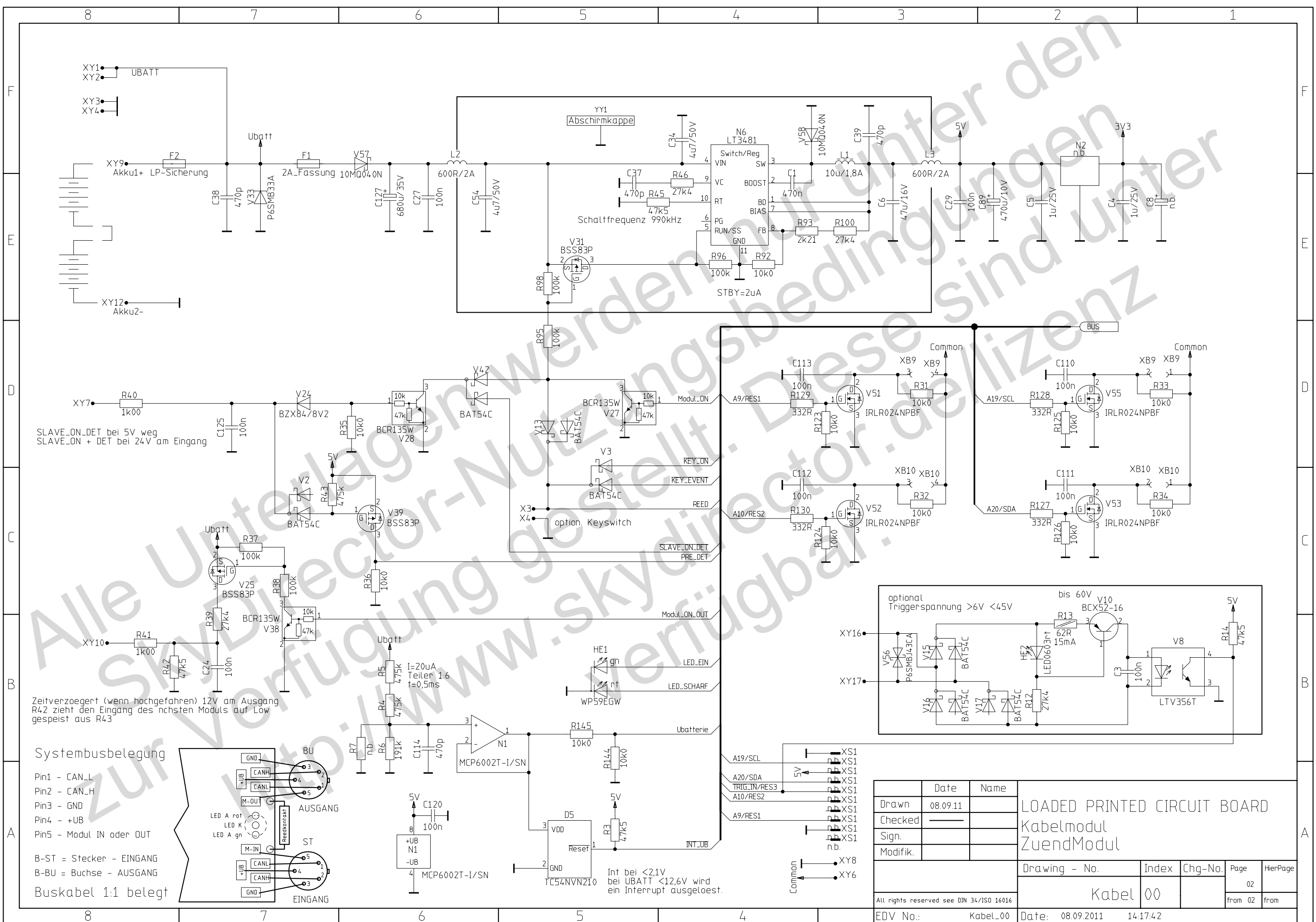
Pin1 - CAN_L
Pin2 - CAN_H
Pin3 - GND
Pin4 - +UB
Pin5 - Modul IN oder OUT

B-ST = Stecker - EINGANG
B-BU = Buchse - AUSGANG
Buskabel 1:1 belegt



CPU		CPU	
PA0	51	PA0/AD0	51
PA1	50	PA1/AD1	50
PA2	49	PA2/AD2	49
Backlight	48	PA3/AD3	47
PA4	47	PA4/AD4	46
PA5	46	PA5/AD5	45
PA6	45	PA6/AD6	44
PA7	44	PA7/AD7	43
A3	10	PB0/SS	10
SCK/KEY_OK	11	PB1/SCK	11
A2	12	PB2/MOSI	12
A1	13	PB3/MISO	13
A11	14	PB4/OC0	14
A12	15	PB5/OC1A	15
A13	16	PB6/OC1B	16
A14	17	PB7/OC2/OC1C	17
STBY	35	PC0/A8	35
STBY_RF	36	PC1/A9	36
RESET_RF	37	PC2/A10	37
A18	38	PC3/A11	38
A17	39	PC4/A12	39
A10/RES2	40	PC5/A13	40
A9/RES1	41	PC6/A14	41
A8	42	PC7/A15	42
Modul_ON_OUT	33	PG0/WR	33
RXD_OFF	34	PG1/RD	34
A7	43	PG2/ALE	43
A15	18	PG3/TOSC2	18
A16	19	PG4/TOSC1	19
RESET	20	PEN	20
XTAL1	24	RESET	20
XTAL2	23	XTAL1	24
AREF	62	XTAL2	23
AVCC	64	AREF	62
AGND	63	AVCC	64
VCC1	21	AGND	63
VCC2	52	VCC1	21
GND1	22	VCC2	52
GND2	53	GND1	22
		GND2	53

	Date	Name	LOADED PRINTED CIRCUIT BOARD Kabelmodul ZuendModul					
Drawn	08.09.11							
Checked	_____							
Sign.								
Modifik.								
			Drawing - No.		Index	Chg-No.	Page	HierPage
			Kabel 00			01		
						from 02	from	
All rights reserved see DIN 34/ISO 16016								
EDV No.:		Kabel_00	Date:		08.09.2011	14:17:42		

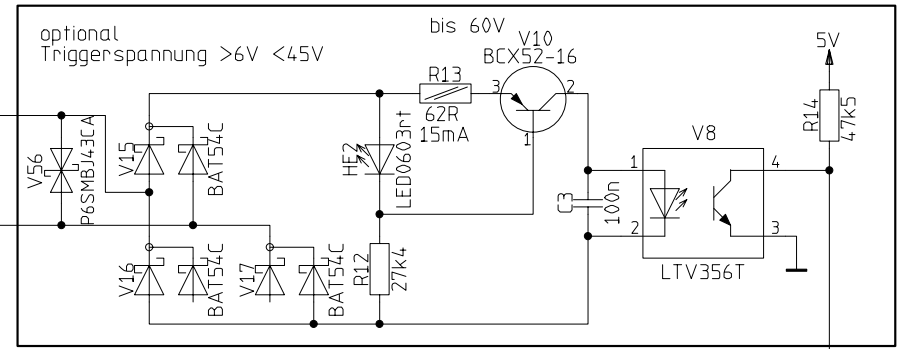
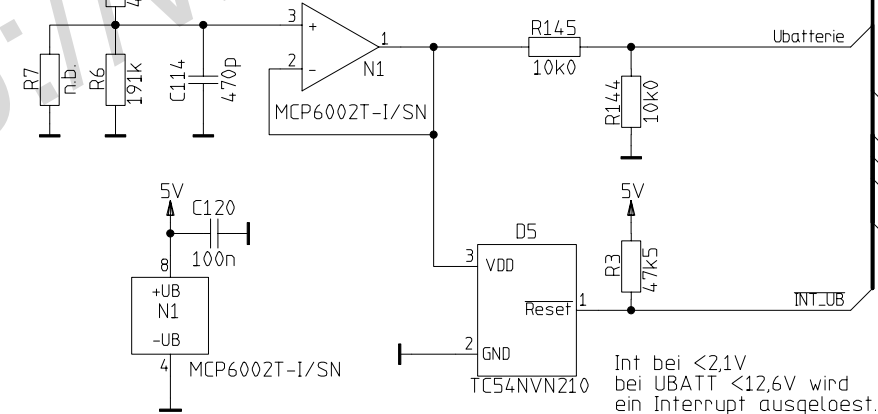
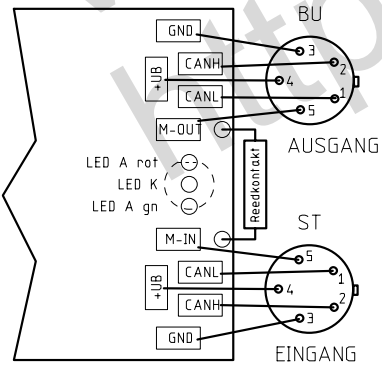


Systembusbelegung

- Pin1 - CAN_L
- Pin2 - CAN_H
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- Pin4 - +UB
- Pin5 - Modul IN oder OUT

- B-ST = Stecker - EINGANG
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Buskabel 1:1 belegt



	Date	Name	LOADED PRINTED CIRCUIT BOARD				
Drawn	08.09.11		Kabelmodul				
Checked			ZuendModul				
Sign.							
Modifik.							
			Drawing - No.	Index	Chg-No.	Page	HierPage
			Kabel 00			02	
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